

REMARKS/ARGUMENTS

Reconsideration of this application as amended is respectfully requested.

Claims 1, 9, 10, 16-18 and 20-22 remain pending in this application, with claims 1, 9, 10, 16 and 18 being independent. Claims 1, 9, 10, 16, 18 and 20 have been amended and claims 2-8, 11-15, 19 and 23-26 have been cancelled.

Applicants would like to thank the Examiner for his indication that claims 6, 9, 14, 16, 17, and 19-22 contain allowable subject matter. Applicants have placed these claims in independent format and believe they are now allowable.

Claims 1, 10 and 18 stand rejected over 35 USC 112, second paragraph. The Examiner rejected these claims because he is not clear on the use of the blocks stored in the temporary instruction cache. Applicants kindly refer the Examiner to at least page 5, lines 11-16 and lines 18-23; page 7, lines 16-19; and page 8, line 7 – page 9, line 22. In one embodiment of the invention having a dual threaded processor, this embodiment may include an IC that handles instructions in blocks that are twice as large as the processing width of the processor. Thus in one clock interval, half of the instruction block is provided to the IQ and the other half of the instruction block is provided to the TIC. On a subsequent clock cycle, the half of the instruction block stored in the TIC is provided to the IQ. This enables outputting the first and second instruction blocks on the same cache access and temporarily storing the second instruction block to provide to an instruction queue on a later clock interval.

In summary, for the reasons noted above, All pending claims are in condition for allowance. It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. Favorable action is respectfully solicited. Allowance of the Claims is respectfully requested.

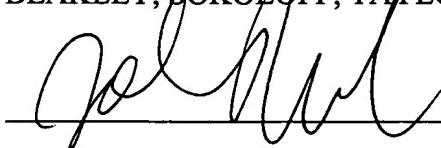
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated:

8/2/04


John Patrick Ward
Reg. No. 40,216

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025